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EXAMINER	
HUISMAN, DAVID J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/037,666	**Applicant(s)** VAJAPEYAM ET AL.	
	Examiner David J. Huisman	**Art Unit** 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2007*.

2a)□ This action is **FINAL**. 2b)☒ This action is non-final.

3)□ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-11,13-15,19-31 and 34-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)□ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,13-15,19-31 and 34* is/are rejected.

7)☒ Claim(s) *35 and 36* is/are objected to.

8)□ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2004 & 03 January 2002* is/are: a)□ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)□ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)□ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)□ All b)□ Some * c)□ None of:

1.□ Certified copies of the priority documents have been received.

2.□ Certified copies of the priority documents have been received in Application No. _____.

3.□ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) □ Notice of References Cited (PTO-892)

2) □ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) □ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) □ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) □ Notice of Informal Patent Application

6) □ Other: _____.

DETAILED ACTION

1. Claims 1-6, 8-11, 13-15, 19-31, and 34-36 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Power of Attorney as received on 3/22/2007 and Extension of Time, RCE, and Amendment as received on 3/26/2007.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of claims 35 and 36 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 36 is objected to because of the following informalities: Please replace "broadcast" with --broadcasted--. Appropriate correction is required.

Withdrawn Rejections

6. Applicant, by way of amendment, has overcome the prior art rejections set forth in the previous Office Action for claims 1 and 10. Consequently, these rejections are hereby withdrawn by the examiner. However, upon further consideration, a new ground(s) of rejection is applied below.

Maintained Rejections

7. Applicant has failed to overcome the prior art rejections set forth in the previous Office Action for claims 20-30. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 28-30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Specifically, claims 28-30 claim a machine-readable medium, and said medium, according to page 18 of applicant's specification, may include a radio frequency (RF) link. Hence, applicant intends the medium of claims 28-30 to include transmission (radio) signals. Consequently, the claims are drawn to a form of energy. Energy is not a series of steps of acts and thus is not a process. Energy is not a physical article or object and as such is not a machine or manufacture. And finally, energy is not combination of substances and therefore not a composition of matter. Since energy is not one of the four categories of invention, claims 28-30 are non-statutory.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 20-22 and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Park, U.S. Patent No. 6,988,190 (as applied in the previous Office Action).

12. Referring to claim 20, Park has taught a method of processing instructions comprising:

a) selecting and fetching a trace descriptor from a tract storage area in accordance with program control flow. See Fig.5 and Fig.6.

b) identifying from the fetched trace descriptor a dependency descriptor including dependency information for a set of instructions and an address of the set of instructions. See Fig.5 and Fig.6. Note that a start address (field 502) of a sequence of instructions as well as dependency information (fields 506 and 508) exists.

c) dispatching the dependency descriptor for execution. After fetching the descriptor, it must be dispatched somewhere for extraction and analysis. This is done for execution of the associated sequence of instructions.

d) fetching the set of instructions from an instruction storage separate from the trace storage area using the address from the dispatched dependency descriptor. Again, field 502 of the descriptor is used to fetch the sequence. It should be noted that the trace cache holds the entries shown in Fig. 6, whereas the instructions themselves are stored in a separate instruction cache (see Fig.2A and column 2, lines 15-16).

e) executing the set of instructions according to dependency information in the dispatched dependency descriptor. See column 4, lines 35-56.

13. Referring to claim 21, Park has taught a method as described in claim 20. Park has further taught updating live-out data in a storage area. Clearly, instructions write result data to some form of memory, whether it be to a stack, to main memory, or to a register file (which is

the most common). The memory written to would hold live-out data, which is data used by subsequent instructions.

14. Referring to claim 22, Park has taught a method as described in claim 20. Park has further taught:

a) storing the identified dependency descriptor from a control flow logic into a storage area. Since the dependency descriptor is updated by "control flow" logic (column 4, lines 35-56), then the control flow logic will store the updates in the address cache.

b) reading the dependency descriptor out of the storage area into the data flow logic. The entries of Fig.5 and Fig.6 are read and used in the execution process.

15. Referring to claim 27, Park has taught a method as described in claim 20. Park has further taught that the selecting comprises predicting a next trace descriptor to process. See the summary of invention section of Park.

16. Referring to claim 28, Park has taught a method of processing instructions comprising:

a) selecting and fetching a trace descriptor in accordance with program control flow. See Fig.5 and Fig.6.

b) identifying from the fetched trace descriptor a dependency descriptor including dependency information for a set of instructions of a dependency chain and an address of the set of instructions, the dependency information to indicate ay least one data on which the dependency chain depends. See Fig.5 and Fig.6. Note that a start address (field 502) of a sequence of instructions as well as dependency information (fields 506 and 508) exists. Note that the set of instructions is dependent on the counter values 506 and 508. Therefore, the set of instructions is a dependency chain of instructions. And, the counter fields indicate at least one data (counter values) on which the dependency chain depends (i.e., the instruction routine's execution is dependent on the counter values).

c) dispatching the dependency descriptor for execution. After fetching the descriptor, it must be dispatched somewhere for extraction and analysis. This is done for execution of the associated sequence of instructions.

d) fetching the set of instructions using the address from the dispatched dependency descriptor. Again, field 502 of the descriptor is used to fetch the sequence.

e) executing the set of instructions according to dependency information in the dispatched dependency descriptor. See column 4, lines 35-56.

17. Referring to claim 29, Park has taught a medium as described in claim 28. Park has further taught that the operations further comprise updating live-out data in a storage area. Clearly, instructions write result data to some form of memory, whether it be to a stack, to main memory, or to a register file (which is the most common). The memory written to would hold live-out data, which is data used by subsequent instructions.

18. Referring to claim 30, Park has taught a medium as described in claim 28. Park has further taught:

a) storing the dependency descriptor in an issue window by control flow logic. The information in the trace descriptor, including the dependency descriptor(s) must be sent somewhere to be analyzed. Since the information causes instructions to be issued, it can be said that an "issue window" holds this information.

b) reading the dependency descriptor out of the issue window into data flow logic. The information must be read to be analyzed.

19. Claims 1-6, 8-11, 13-15, 19, 31, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al., U.S. Patent Application Publication No. US 2002/0144101 (as cited by applicant and herein referred to as Wang).

The applied reference has a common assignee and inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

20. Referring to claim 1, Wang has taught a logic circuit comprising:

a) data flow logic. See the pipeline of Fig.1.

b) control flow logic to select and fetch a trace descriptor for processing, the fetched trace descriptor including at least one dependency descriptor, the control flow logic to dispatch to the data flow logic a dependency descriptor including dependency information having live-in information and live-out information for an instruction sequence and an address of the instruction sequence. See the abstract and Fig.1. Trace descriptors include dependency descriptors which further include live-in and live-out information, according to the embodiment disclosed in paragraph [0036]. The dependency descriptor also has instruction sequence address information according to an embodiment. See paragraph [0020].

c) the data flow logic coupled to the control flow logic to receive the dispatched dependency descriptor, to fetch the instruction sequence using the address from the received dependency descriptor, and to execute the instruction sequence according to the dependency information in the received dependency descriptor. See the abstract and paragraph [0036].

21. Referring to claim 2, Wang has taught a logic circuit as described in claim 1. Wang has further taught a storage area coupled to the control flow logic and the data flow logic, the storage area to store the dependency descriptor from the fetched trace descriptor by the control flow logic. See Fig.1 and paragraph [0036], and note that the trace cache (storage area) holds the dependency information.

22. Referring to claim 3, Wang has taught a logic circuit as described in claim 1. Wang has further taught a storage area coupled to the control flow logic, the storage area to store trace descriptors. See Fig.1, component 22.

23. Referring to claim 4, Wang has taught a logic circuit as described in claim 3. Wang has further taught a second storage area coupled to the data flow logic, the second storage area to store instructions contiguously based on dependency information. See Fig.1, component 14. Also note that instruction are inherently stored contiguously based on dependency information. That is, dependent instructions follow instructions which they are dependent on. This is the inherent nature of dependency.

24. Referring to claim 5, Wang has taught a logic circuit as described in claim 1. Wang has further taught a storage area coupled to the data flow logic and control flow logic, the storage area to store live-out data. See Fig.1, component 22, and paragraph [0036].

25. Referring to claim 6, Wang has taught a logic circuit as described in claim 1. Wang has further taught a storage area coupled to the control flow logic, the storage area to map dependency information. See Fig.1, component 22 and note that dependency information is

mapped to a certain instruction trace by being stored with information defining the locations of the instruction trace.

26. Referring to claim 8, Wang has taught a logic circuit as described in claim 1. Wang has further taught that the trace descriptor includes aggregate live-in data for a plurality of dependency descriptors in the trace descriptor. See paragraph [0036].

27. Referring to claim 9, Wang has taught a logic circuit as described in claim 1. Wang has further taught that the trace descriptor includes aggregate live-out data for a plurality of dependency descriptors in the trace descriptor. See paragraph [0036].

28. Referring to claim 10, Wang has taught a computer system comprising:

a) at least one memory device to store trace descriptors and instruction sequences, each trace descriptor associated with a trace. See Fig.1, components 14 and 29, and the abstract.

b) a bus coupled to the at least one memory device. See Fig.1 and Fig.2 and also note that a bus must inherently exist if data/instructions are to be retrieved from the memory device(s).

c) control flow logic to select and fetch one of the trace descriptors, the fetched trace descriptor including aggregate live-in information and aggregate live-out information for the corresponding trace, a plurality of dependency descriptors having locations of corresponding instruction sequences within the trace and having dependency information for the corresponding instruction sequences. See the abstract and Fig.1. Trace descriptors include dependency descriptors which further include live-in and live-out information, according to the embodiment disclosed in paragraph [0036]. The dependency descriptor also has instruction sequence address/location information according to an embodiment. See paragraph [0020].

d) data flow logic coupled to the control flow logic to receive a dependency descriptor dispatched from the control flow logic, to fetch an instruction sequence corresponding to the received dependency descriptor, and to execute the fetched instruction sequence according to dependency information in the received dependency descriptor. See the abstract, the pipeline of Fig.1, and paragraph [0036].

29. Referring to claim 11, Wang has taught a computer system as described in claim 10. Wang has further taught an issue window coupled between the control flow logic and the data flow logic, the issue window to store the dependency descriptor dispatched from the control flow logic. The information in the trace descriptor, including the dependency descriptor(s) must be sent somewhere to be analyzed. Since the information causes instructions to be issued, it can be said that an "issue window" holds this information.

30. Referring to claim 13, Wang has taught a computer system as described in claim 10. Wang has further taught that the at least one memory device is to store an instruction sequence contiguously based on dependency information. See Fig.1, component 14. Also note that instruction are inherently stored contiguously based on dependency information. That is, dependent instructions follow instructions which they are dependent on. This is the inherent nature of dependency.

31. Referring to claim 14, Wang has taught a computer system as described in claim 10. Wang has further taught a storage area coupled to the data flow logic and control flow logic, the storage area to store live-out data. See Fig.1 and paragraph [0036].

32. Referring to claim 15, Wang has taught a computer system as described in claim 10. Wang has further taught a storage area coupled to the control flow logic, the storage area to map

dependency information. See Fig.1, component 22 and note that dependency information is mapped to a certain instruction trace by being stored with information defining the locations of the instruction trace.

33. Referring to claim 19, Wang has taught a computer system as described in claim 10. Wang has further taught that dependency information in the received dependency descriptor includes live-in and live-out data. See paragraph [0036].

34. Referring to claim 31, Wang has taught a logic circuit as described in claim 1. Wang has further taught that the fetched trace descriptor includes a plurality of dependency descriptors having addresses of corresponding instruction sequences and having dependency information for corresponding instruction sequences. See Fig.3A-5. Note that each pair of instructions in an overall instruction sequence (represented by a DAG) is itself an instruction sequence for which dependency information exists. Paragraph [0036] also discloses that an address of a second sequence can be encoded into the trace (next trace field).

35. Referring to claim 34, Wang has taught a computer system as described in claim 10. Wang has further taught that the data flow logic includes a plurality of clusters each to independently execute different fetched instruction sequences each corresponding to a different received dependency descriptor. See Fig.2, and note that multiple pipelines (clusters) exist. The first pipe executes a first sequence and the second pipe executes a second sequence.

Claim Rejections - 35 USC § 103

36. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

37. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Arimilli et al., U.S. Patent No. 6,427,204 (as applied in the previous Office Action and herein referred to as Arimilli).

38. Referring to claim 23, Park has taught a method as described in claim 20. Park has not taught that the fetching of a set of instructions is completed just in time for execution. However, Arimilli has taught such a concept. See column 3, lines 1-17. Note that Arimilli has taught that this is a more efficient way of fetching because instructions are only delivered when they are actually needed and pipeline bubbles are prevented. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Park such that instructions are fetched just-in-time, as taught by Arimilli.

39. Referring to claim 24, Park has taught a method as described in claim 20. Although Park has not taught that the instructions are out of order, Arimilli has taught such a concept. See column 1, line 61, to column 2, line 6. Note that the use of resources and efficiency are maximized with out-of-order execution. In addition, out-of-order execution allows for a reduction in stalling. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Park to include instructions that are out-of-order, as taught by Arimilli.

40. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Witt et al., U.S. Patent No. 6,018,798 (as applied in the previous Office Action and herein referred to as Witt).

41. Referring to claim 25, Park has taught a method as described in claim 21. Park has not explicitly taught updating the architectural state using the data in the storage area. However, Witt has taught the concept of having a speculative register file (future file 88, Fig.3) and an actual register file (Fig.3, component 102). The speculative register file holds the most current state of the machine (values determined via speculative execution) and by doing this, instructions may be executed speculatively. Once it is determined that instructions are no longer speculative, the speculative results are made architectural results by writing them to the actual register file. See column 12, line 66, to column 13, line 45. This is a known concept in the art. In essence, this scheme allows for speculative execution which is a method of executing instructions before it is known that they should execute (they are predicted to execute). This maximizes efficiency if they indeed were to execute (predicted correctly). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Park such that the architectural state is updated using the data in the speculative storage.

42. Referring to claim 26, Park in view of Witt has taught a method as described in claim 25. Witt has further taught recovering an earlier architectural state after a misprediction using data in the storage area. See column 18, lines 54-67, and note that after a misprediction, a previous state is achieved by copying actual values into the future file (so that the speculative values are correct). Consequently, by using this newly written data, the system recovers an earlier architectural state.

Allowable Subject Matter

43. Claims 35-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

44. Applicant's arguments filed on March 26, 2007, have been fully considered but they are either moot or not persuasive.

45. Applicant's arguments with respect to claims 1 and 10, and any associated dependent claims, have been considered but are moot in view of the new ground(s) of rejection.

46. Applicant argues the novelty/rejection of claim 20 on page 9 of the remarks, in substance that:

> "As to claim 20, Park nowhere teaches selecting and fetching a trace descriptor from a trace storage area and fetching an instruction set from an instruction storage separate from this trace storage area. Instead, in Park the address trace cache 220 includes address information, iteration information, as well as the routines, as shown in FIG. 5 of Park. Accordingly, claim 20 and the claims depending therefrom are patentable."

47. These arguments are not found persuasive for the following reasons:

a) Park has clearly disclosed separate storage areas for traces and instructions. Specifically, Fig.2A and column 2, lines 15-16 disclose an instruction cache in which instructions are stored. Fig.2B and column 2, lines 16-27, on the other hand, disclose a trace cache for storing traces. The idea behind Park is to conserve trace cache area (see the title) and therefore instead of storing instructions in the trace cache, Park stores start and end addresses of a set of instructions to be executed (see Fig.5, fields 502 and 504). When the trace entry is fetched from the trace cache, the start and end addresses are used to access the instruction routine from the instruction cache. The examiner asserts that Fig.5 does not show that the instructions are stored with the trace information. Fig.5 merely shows that the start and end addresses point to start and end addresses of instruction routines.

48. Applicant argues the novelty/rejection of claim 28 on page 9 of the remarks, in substance that:

> "As to independent claim 28, Park nowhere teaches the presence of a dependency descriptor that includes dependency information to indicate at least one data on which a dependency chain depends. Instead, as described above the Office Action appears to contend that the recited dependency information is the iteration counts. However, such iteration counts nowhere indicate "data" on which a dependency chain depends. Accordingly, claim 28 and the claims depending therefrom are patentable."

49. These arguments are not found persuasive for the following reasons:

a) The count fields do indicate a count value. The execution of the dependency chain, i.e., the instruction routine, is dependent on the count value because when the count has reached its limit, the routine will no longer execute. Until that point, however, the routine will execute.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
David J. Huisman
May 30, 2007